

quantumdata[™] 980 HDMI Phy & Protocol Aux Chan Analyzer Module HDMI 2.0 CEC Compliance



Key Features

- Run HDMI 2.0 CEC Compliance tests
- Test HDMI DDC bus characteristics such as bit timing, pull-up resistance and low level voltage
- Pre-test or self-test your HDMI
 2.0 CEC capable devices to reduce costs and improve time to market
- Run tests individually or in batch; reuse stored test configurations
- Share your compliance test results with colleagues and subject matter experts
- Provides access to HDMI auxiliary channel pins for direct measurements

The quantumdata 980 HDMI 2.0 Phy & Protocol Aux Channel Analyzer module is equipped with an HDMI Tx port and an HDMI Rx port for running tests on HDMI auxiliary channels such as the DDC channel and the CEC bus. The 980 Phy & Protocol Aux Channel Analyzer module's CEC compliance tests enable you to identify compliance failures early in the development cycle. The solution is ideal for pre-testing and self-testing (where permitted) your HDMI 1.4 & 2.0 device.

Compliance Tests

The 980 Phy & Protocol Aux Channel Analyzer module's HDMI CEC compliance tests enable you to identify compliance failures early in the development cycle. Pre-testing and self-testing reduces cost of testing or retesting at an Authorized Test Center (ATC) and enables you to meet time to market requirements. You can save the results and distribute them to colleagues.

Operation

The 980 HDMI Phy and Protocol Aux Channel Analyzer module's compliance tests can be controlled either through the PC-based 980 GUI Manager or through the embedded 980 GUI Manager running on the 980 platform itself. The 980's built-in color touch screen provides a graphical user interface (GUI) to control the module and run the compliance tests.

HDMI 2.0 CEC COMPLAINCE TESTING

CEC Compliance Testing

The 980 CEC compliance tests are ideal for pre-testing your product prior to submission to an Authorized Test Center for approval. Pre-testing provides added assurance that your product will pass at the Authorized Test Center (ATC) when submitted.

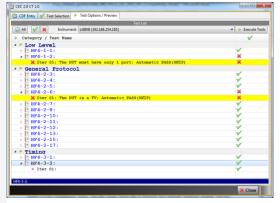
HDMI 2.0 Compliance Tests

The 980 HDMI Phy & Aux Channel Protocol Analyzer supports various CEC compliance tests (MOIs) for HDMI 2.0 CTS Sections 10.1, 10.2 and 10.3.

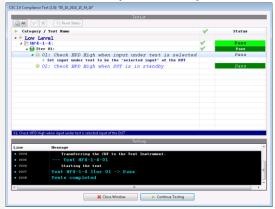
HDMI 2.0 CEC Test Selection

5 CEC 20 CT 20	
CDF Entry 🗸 Test Selection 🕨 Test Options / Preview	
🕰 Open 🔣 Save 🛛 🗷 Select All Tests on Page 🔛 Deselect All Tests on Page	
▶ Tests (16/26)	
► HF4-1 Low Level 2	7 🖬
► HF4-2 General Protocol 12	17 🖬
▶ HF4-3 Timing 2	2
HF4-2-1 Ensure all basic CEC commands that are marked as mandatory for the DUT are implemented and work correctly. HF4-2-2 HF4-2-2	Î
Check if the DUT ignores applicable messages sent from LA=15.	
PIF4-2-3 Verify that the DUT responds with <feature abort=""> for all unsupported opcodes that are directly addressed.</feature>	1
HF4-2-4 Verify that the DUT ignores all unsupported opcodes that are broadcast.	
IF4-2-5 Veryfy that the device interprets a CEC message with additional operands. (This test spelles if the EUUT is a TV)	
✓ HF4-2-6 Verify that the device interprets a CIC message with additional operands. (This test applies if the OUT is not a Th)	
HF4-2-7 Verify that the DUT adheres to the mandatory message dependencies of the CEC specification as a Follower.	
HF4-2-8 Verify that the DUT adheres to the mandatory message dependencies of the CEC specification as an initiator.	Close

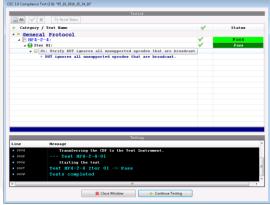
HDMI 2.0 CEC Test List

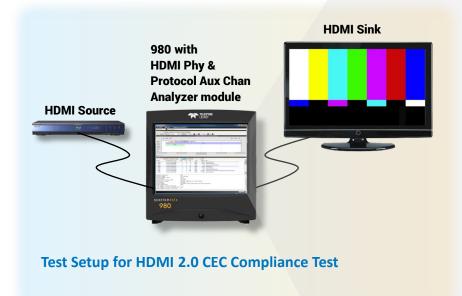


HDMI 2.0 CEC Compliance - Sample Results



HDMI 2.0 CEC Compliance - Sample Results





Self-Testing

Where permitted, the 980 HDMI Phy & Aux Channel Protocol Analyzer can be used to self-test your product. Self-testing offers greater benefits for time to market and cost reduction than pre-testing by avoiding submission to the Authorized Test Center (ATC) for approval.

Test Results

The compliance tests provide detailed test results which help pinpoint the cause of compliance test failures.

DDC CHANNEL TEST FEATURES

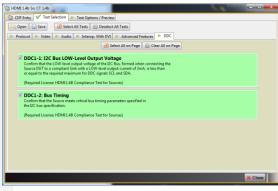
DDC Channel Testing

The 980 HDMI Phy & Aux Channel Protocol Analyzer module supports previously untested characteristics of the HDMI 1.4b DDC channel. You can run tests on the HDMI DDC bus on source and sink devices. Tests include Low level output voltage, bus timing and pull-up resistance.

Test Results

Detailed test results enable you to pinpoint the cause of compliance test failures.

Tests Available for HDMI DDC Sink Sources



980 with HDMI Phy & Protocol Aux Chan Analyzer module



Test Setup for DDC Bus Source Tests



Test Setup for DDC Bus Sink Tests

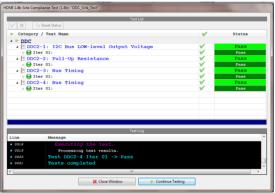
Test Results - DDC Channel Source Tests

Test Name / Details	0	Status
DDC1-1: I2C Bus LOW-Level Output Voltage	-	Pass
4 😝 Iter 01:		Pass
01: 6.2 Verify Source start a DDC transaction		Pass
		Pass
03: 7.4 Verify VOL SCL < 0.4V		Pass
DDC1-2: Bus Timing		Pass
4 😔 Iter 01:		Pass
01: 8 Verify Source start a DDC transaction		Pass
02: 9.1 Verify no occurrence of t HD;STA < 4.0us		Pass
03: 9.2 Verify no occurrence of t SU;STA < 4.7us		Pass
04: 9.3 Verify no occurrence of t SU;STO < 4.0us		Pass
05: 9.4 Verify no occurrence of t BUF < 4.7us		Pass
06: 9.5 Verify no occurrence of t HD;DAT < Ous		Pass
07: 9.6 Verify no occurrence of t SU;DAT < 250us		Pass
o ∲ Open Cacture DDCI-1: DC Rvs LOW-Level Output Voltage		

Tests Available for HDMI DDC Sinks

HDMI 14b Sink CT 14b	×
CDF Entry V Test Selection > Test Options / Preview	
📴 Open 🔛 Save 🛛 Select All Tests 📄 Deselect All Tests	
EDID / E-DDC Protocol Video Audio Interop. with DVI Advanced Features DDC	
Select All on Page	
✓ DDC2-1: 12C Bus I/OW-level Output Voltage Confirm that the UV-level output voltage of the UC Bus, formed when connecting the Sin 20 UT is a compariar Source configures to not a UV-level output current of JanA results in a X dis 3.6 X/h, loss than or equal to the required maximum V_of for the UCC Sol signal.	
(Required License: HDMI 1.48 Compliance Test For Sinks)	
DOC2-2: Pull-Up Resistance Codem that the Sink pull-up existance meets the minimum requirements for DDC against SCL and SAN. (Required Licence: HCM1148 Compliance Test For Sinks)	
DDC2-3: Bus Timing Confirm that the Silv nearth the step and hold bus timing parameters specified in the IZ-bus specification when driving the SDA signal. Required Linear Hold LiAC Configurations: Test for Sinkal	
(required ancested internative comparated react or onney)	
DDC2-4: Bus Timing Confirm that the Sink does not require more setup or hold time than specified in the IIC bus specification when reading the SDA signal.	
(Required License: HDMI 1.4B Compliance Test For Sinks)	
¥ Close	T

Test Results - DDC Channel Sink Tests



SPECIFICATIONS

HDMI Ports

Version	HDMI 1.4x & 2.0x
Standard Formats	VESA, CEA
Connector	Type A Tx & Rx
Protocol	HDMI
Video Colorimetry	ITU-R BT.601-5, ITU-R BT.709-5
Video Max Pixel Rate	300MHz (300 Gbps/channel TMDS rate)
Color Depths	8, 10, 12 bits
Video Encoding	RGB, YCbCr
Video Sampling Modes	4:4:4, 4:2:2, 4:2:0

Compliance Test Support

HDMI 2.0 CEC Tests	Various CEC tests in Sections: 10.1, 10.2 and 10.3 of the HDMI 2.0 Compliance Test Specification
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Options

Compliance Test Package #7	See list in table above

Aux Connectors

980B Test Platform

Embedded Display	15" diagonal; Resolution: 1024(H); x 768 (V) resolution; 24 bit RGB color.
Power	90-264 VAC, 47-63Hz
Weight	23.76 LBS; 10.78 Kg
Size	Height: 15.25 in. (38.7 cm) Width: 14.57 in. (36.5 cm) Depth: 6.29 in. (15.9 cm)
Command Line Control	Ethernet (RJ-45) for external GUI and telnet
Environmental	Operating Temp: 32 to 104 (F); 0 to 40 (C)







Local sales offices are located throughout the world. Visit our website to find the most convenient location.